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Design of Low Power Successive Approximation Analog to Digital Converter

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Abstract
In Biomedical applications such as pacemaker it becomes mandatory to design the circuits with low power and low voltage to enhance the system by means of long sustainability and less power consumption with maintenance free operation, especially in the circuits like Analog to Digital Converters (ADCs). So here is the selection of right architecture is very crucial. Day by day more and more applications are built on the basis of power consumption so SAR ADC will be useful for medium speed with medium resolution and low power consumption. This SAR ADC is designed in Tanner Tool V13.0 . This is implemented in 180 nm technology.
Keywords: Successive Approximation Register (SAR), Low power, Resolution, Pacemaker.

I. INTRODUCTION

Analog to Digital Converters are important building blocks in lots of applications. In past few years, more and more applications are built with very stringent requirements on power consumption. For electronic systems, such as wireless systems or implantable devices, the power consumption is becoming one of the most critical factors. The stringent requirements on the energy consumption increase the need for the development of low voltage and low power circuit techniques and system building blocks. Analog-to-Digital Converters (ADCs) translate the analog quantities into digital language, used in information processing, computing, data transmission and control systems. ADCs are key components for the design of power limited systems, in order to keep the power consumption as low as possible. Implantable Medical electronics, such as Pacemakers and cardiac defibrillators are typical examples of devices where ultra-low-power consumption is paramount .The implanted units rely on a small non rechargeable battery to sustain a lifespan of upto 10 years. The life time of the artificial pacemakers should last up to 10 years which mandate low power consumption per operation. The analog to digital converter is the crucial part of an implantable pacemaker since it consumes a large amount of power as the interface between sensed analog signal and digital signal processor block.

Low power ADCs with moderate resolution and low sampling frequency is suited for biomedical application. These specifications make SAR ADC the suitable choice. It consumes low power due to its simple structure. Moreover, SAR ADC is scalable with the technology scaling since most parts of the architecture apart from the comparator are digital.

The rest of the paper is organized as follows; one biomedical device Pace Maker operation is explained in Section II. The SAR ADC architecture operation is explained in Section III….

II. PACEMAKER OPERATION

Pacemakers directly control the pattern and speed of the heartbeat. When the heart stops beating or it beats too slowly, pacemaker provides weak electrical signals with approximately 70 beats per minute to correct the timing of the heart beat. This medical device contains a battery, a generator and pacing leads. The leads connect the pacemaker to the heart and stimulate the heart with the pulses generated in pacemaker. Battery and generator are inside a titanium container which is placed inside the body. Figure shows the block diagram of a pacemaker. The main blocks fall into four parts

1) At the input, there are sensing system, amplifier, filter, and analog to digital converter.
2) The digital output of the ADC is fed to the logic block.

This consists of a programmable logic, timing control system and therapy algorithms.

3) Current and voltage reference generator and battery power management.
4) At the output of the pacemaker, high voltage pulse generator and multiplier exist.[2]

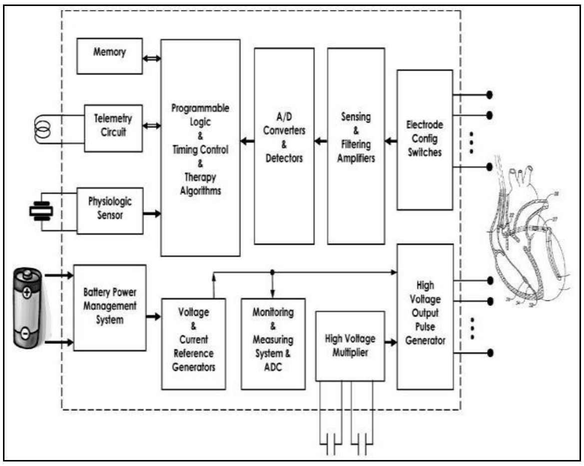

Figure 1. Pacemaker functional blocks

III. PROPOSED ARCHITECTURE OF SUCCESSIVE APPROXIMATION ADC

Successive approximation register (SAR) ADC is designed based on a binary search algorithm. It consists of a successive approximation register (SAR), a digital-to-analog converter and a comparator which is illustrated in Fig.2. First, input voltage (Vin) is given to inverting terminal of comparator and the registers are reset to zero. secondly, the conversion starts through an approximation of MSB (set MSB as one) by SAR; DAC converts the digital information to a voltage Vout (half of the reference voltage Vref). Comparator compares V_d with Vin. If Vin is larger than V_d it outputs '1', otherwise, it outputs '0'; SAR loads the comparator result, registers the value of MSB and generates its next approximation; the conversion continues until the LSB is decided. Therefore, an N -bit SAR ADC needs N clock cyc1es per conversion. SAR ADC is known for its simple structure, thus consuming less power and saving more die size. However, with increase of its resolution, the linearity problem of DAC becomes more severe, which directly causes non linearity of ADC. Therefore, SAR ADC is not suitable for high resolution.[2]

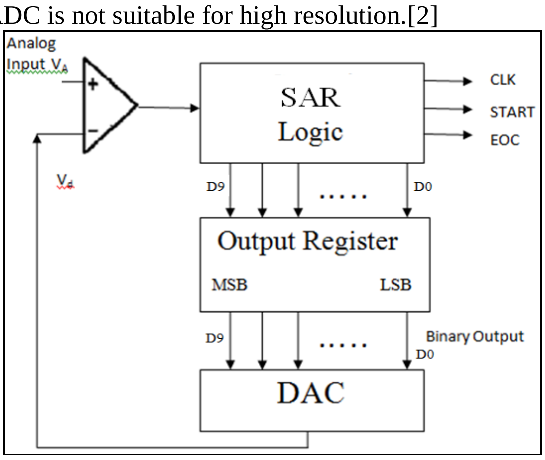

Figure 2. Block diagram of a SAR ADC

A) DIGITAL TO ANALOG CONVERTER

The digital to analog converter (DAC) converts the digital word at the output of the SAR logic to an analog value. Then in the comparator, this value is compared to the input signal. The Digital to Analog Converter has a resolution of 10 bits. In this Degrading Capacitor technique is used which consist of 10 Capacitors which are arranged in a fashion of Binary weighted type. In this MSB capacitor having highest value of 512 uf and then next capacitor having value just half of the above and so on till LSB Capacitor. 10 Bit digital input which is nothing but the output of SAR logic are giving to respective capacitors through inverter.

B) COMPARATOR

The comparator is an essential part in the SAR ADC to perform the binary search algorithm. Comparator in the SAR ADC takes more power consumption than the other blocks. A comparator generates a logic output high or low based on the comparison of the analog input with a reference voltage. In an ideal comparator, with infinite gain, for input voltages higher than the reference voltage, the comparator outputs logical one and for the input voltages lower than the reference voltage it produces zero at the output.

C) SAR LOGIC

Successive Approximation Register (SAR) control logic determines each bit successively. The SAR register contains N bit for an N-bit ADC. There are 3 possibilities for each bit, it can be set to ‘1’, reset to ‘0’ or keeps its value. In the first step, MSB is set to ‘1’ and other bits are reset to ‘0’, the digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared to the input. Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output of the DAC, the MSB remains at ‘1’, otherwise it is reset to ‘0’. The rest of bits are determined in the same manner. In the last cycle, the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+1 clock cycles to perform a conversion. Successive approximation register ADC implements the binary search algorithm using SAR control logic.

IV. EXPERIMENTAL RESULTS & DISCUSSION

SAR ADC is known for its simple structure, thus consuming less power consumption as compared to other ADC’s. Therefore, SAR ADC is not suitable for high resolution. The sub blocks of SAR ADC design and results will be shown below.

A) **Digital To Analog Converter**

As there are different techniques for converting a digital signal into an analog signal representation. The approaches differ in speed, power efficiency, achievable accuracy, etc. It is therefore necessary to understand which converter algorithms or architectures to choose for the specific application In this Degrading Capacitor technique is used which consist of 10 Capacitors which are arranged in a fashion of Binary weighted type. In this MSB capacitor having highest value of 512 uf and then next capacitor having value just half of the above and so on till LSB Capacitor. 10 Bit digital input which is nothing but the output of SAR logic are giving to respective capacitors through inverter.

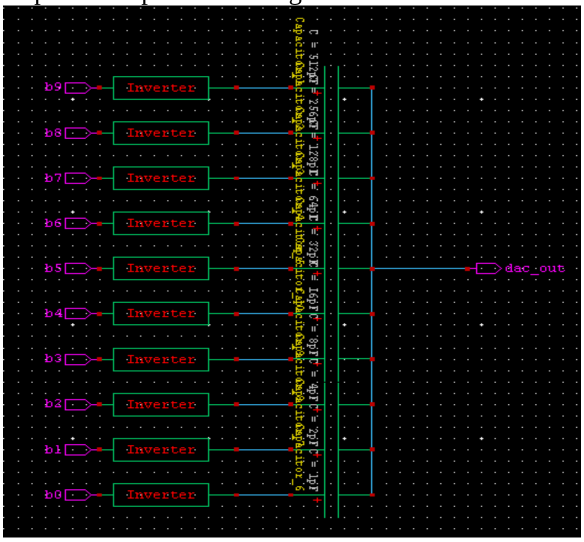

Figure 3. Design of 10-Bit Digital to Analog Converter

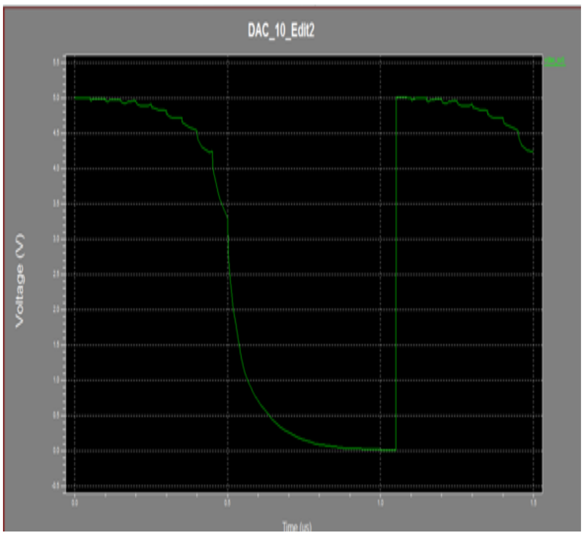

Figure 4. Output of DAC

B) **Comparator**

A comparator generates a logic output high or low based on the comparison of the analog input with a reference voltage. The comparator in the SAR ADC takes more power consumption than other blocks. In SAR ADC we must design comparator such that it consumes very less power. In the Figure5. V_{in} given to the -ve terminal and the V_{ip} given to the +ve terminal of comparator, when $V_{ip} > V_{in}$ the output is high and low when $V_{ip} < V_{in}$.

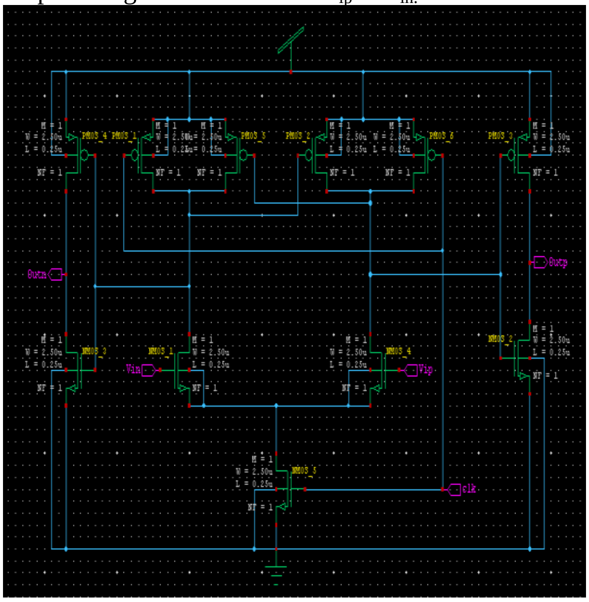

Figure 5. Design of Comparator

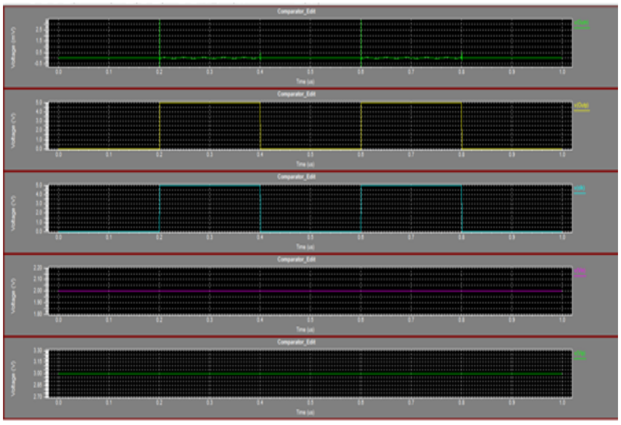

Figure 6. Output waveform of Comparator

C) **SAR Logic**

This SA register contains 10 bit for an 10-bit ADC. In the first step, MSB is set to 1 and other bits are reset to 0, the digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared with the input. Based on the comparator result, this SAR controller defines the MSB value. If the input is higher than the output of the DAC, the MSB remains at 1, otherwise it is reset to 0. The rest of bits are determined in the same manner. In the last cycle, the converted digital word is stored. Therefore, an 10-bit SAR ADC takes 11 clock cycles to perform a conversion. The SAR logic consist of counter which made using D-flip flop.

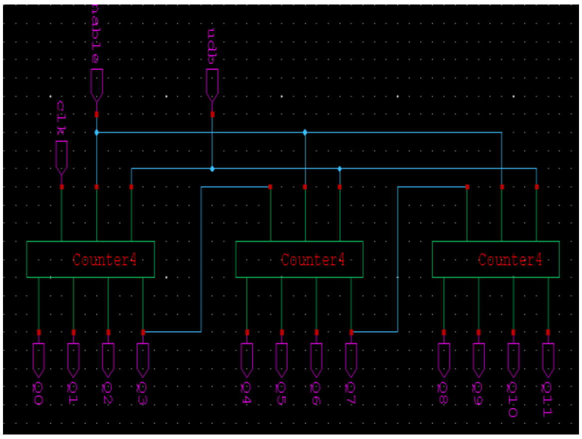

Figure 7. Design of SAR Logic

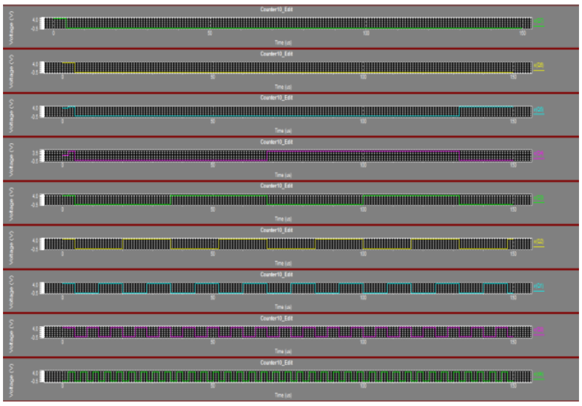

Figure 8. Output waveform of SAR Logic

D) **SAR ADC Design:**

Fig.9 shows the design of 10 bir SAR ADC which consist of 10-bit DAC, Comparator and then SAR logic. The design and simulation result of each block is shown above. Here comparator Comparator compares the input voltage V_{in} with the analog output of DAC then this output of comparator given to SAR logic and then output of SAR logic given to input of DAC. Here, power consumption of ADC is mainly depend on performance of comparator.

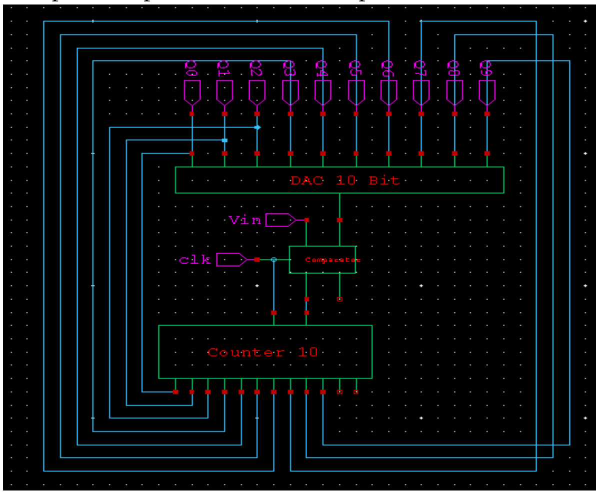

Figure 9. Design of SAR ADC

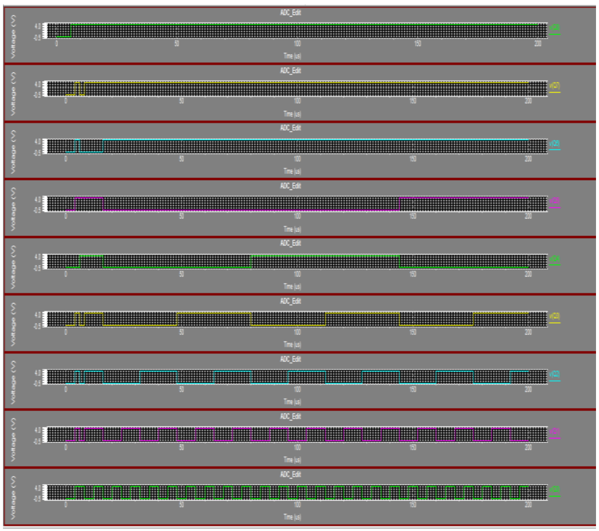

Figure 10. Output of SAR ADC

V. CONCLUSION

A successive approximation ADC is suitable for operation at ultra low supply voltage is realized in a 0.18um CMOS technology using standard threshold CMOS devices . This SAR ADC is well suited for biomedical applications such as Pacemaker, MRI, ECG and EEGs.

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